a metal wiring layer provided on said active element;

an interlayer insulating film covering said active element;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film; and

a barrier metal layer provided on said active element with said interlayer insulating film therebetween, so that said pad metal is provided on said barrier metal layer and covering said active element, wherein:

said interlayer insulating film has at least a level difference compensating film for compensating a level difference of the metal wiring layer; and

a portion of said level difference compensating film under said pad metal is removed.

15. (Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a metal wiring layer provided on said active element;

an interlayer insulating film covering said active element;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film; and

a barrier metal layer provided on said active element with said interlayer insulating film therebetween, so that said pad metal is provided on said barrier metal layer and covering said active element,

wherein:

said interlayer insulating film has at least a level difference compensating film for compensating a level difference of the metal wiring layer; and

said level difference compensating film is formed to a minimum thickness necessary for compensating the level difference of the metal wiring layer.

16. (Amended) A semiconductor device as set forth in claim 14, further comprising a passivation film, said passivation film being formed so as to cover a large part of said pad metal, and an aperture in said passivation film having an edge adjacent an inside edge of said pad metal.

22. (Twice Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a lower interlayer insulating film formed so as to cover said active element;

a metal wiring layer provided on said lower interlayer insulating film;

an upper interlayer insulating film formed so as to cover said metal wiring layer; and

a pad metal for an electrode pad, said pad metal being provided on said upper interlayer insulating film and covering said active element,

another metal wiring layer formed on the active element;

wherein each of said lower and upper interlayer insulating films have a trilaminar structure, each of a first layer and a third layer of the trilaminar film being a silicon

nitride film or a silicon oxide film, while a second layer of the trilaminar film being formed of spin-on-glass;

and the second layer of the upper interlayer insulating film formed to a minimum thickness necessary for compensating the level difference of the metal wiring layer.

25. (Twice Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a first metal wiring layer formed on the active element;

a plurality of other metal wiring layers above said active element; and

a plurality of interlayer insulating films each being provided between a pair of said plurality of other metal wiring layers,

wherein each interlayer insulating film has a multilayer structure including at least a spin-on-glass film sandwiched between insulating films formed of a silicon nitride film or a silicon oxide film;

further wherein the film formed of spin-on-glass in the interlayer insulating film being formed to a minimum thickness necessary for compensating a level difference of one of said plurality of other metal wiring layers;

a pad metal for an electrode pad, said pad metal being provided on said interlayer insulating film.

Add the following new claims 26 and 27.